IN THE CLAIMS:

Please **amend claim 1** as indicated below, and **add claims 13-16** follows:

1. (*Currently amended*) A content addressable memory comprising a CAM control logic unit and a plurality of cells connected in a chain, the cells being serially connected, each of the cells including:

a memory block;

a data interface and a plurality of addresses arranged to be sequentially addressed through the data interface, the plurality of addresses being coupled to a common address bus;

a comparator coupled to a common data bus and to the data interface of the memory block;

a switch for coupling the data interface of the memory block with the data bus; and

a logic block including a Match flip-flop;

the memory being ~~operable~~ arranged to have a search phase and an access phase so that:

(a) in ~~a Search~~ the search phase, ~~to serially match~~ a sequence of words on the common data bus is matched with the contents of a sequence of addresses in the memory blocks of the cells~~, the logic block being arranged for cumulatively storing the results of the matching as the matching proceeds~~; and

(b) in ~~an Accese~~ the access phase, ~~to render~~ causing the cells matched in the ~~Search~~ search phase to be serially available for access via the common address and data buses, said ~~Accees~~ access phase occurring subsequent to said ~~Search~~ search phase,

the logic block being arranged for cumulatively storing the results of the serial matching during the memory search phase as the matching proceeds.

2. (*Previously presented*) A content addressable memory according to claim 1 wherein each cell includes a memory block, a logic block, a comparator, and a bidirectional switch.

3. (*Previously presented*) A content addressable memory according to claim 1 wherein an integrated circuit chip carries the CAM and plural cells.

4. (*Previously presented*) A content addressable memory according to claim 3 wherein several of the chips are chained.

5. (*Original*) A content addressable memory according to claim 4 wherein each chip includes a control unit which can be disabled.

6. (*Previously presented*) A content addressable memory according to claim 1 including a MASK bus input for determining which bits of the words of the sequence of words are used for matching in the Search phase.

7. (*Previously presented*) A content addressable memory according to claim **1** including a return line from the end of the chain of cells back to the CAM control unit for changing state in response to all Match flip-flops in the chain having been accessed.

8. (*Previously presented*) A method of operating a content addressable memory according to claim **1** comprising the steps of choosing a standard byte address in all data blocks and including a byte different from the inactive state of the data bus in that address in every data block.

9. (*Previously presented*) A method of operating a content addressable memory according to claim **1** wherein each cell is divided into a plurality of distinct data blocks.

10. (*Previously presented*) A method of operating a content addressable memory according to claim **1** wherein a plurality of cells are combined into an extended data block with all cells of the block including corresponding key fields.

11. (*Previously presented*) A method of operating a content addressable memory according to claim **1** further including choosing a standard byte address in all data blocks and filling the data blocks with one data value if the data block in that cell is valid and another data value if the data block in the cell is cleared.

12. (*Cancelled*)

13. (*New*) A method of operating a content-addressable memory having a search phase and an access phase, the memory including a CAM control logic unit and a plurality of cells connected in a chain, the cells being serially connected, each of the cells including a memory block comprising a data interface and a plurality of addresses sequentially addressable through the data interface and coupled to a common address bus, the method comprising:

(a) serially matching, during the search phase, a sequence of words on the common data bus with the contents of a sequence of addresses in the memory blocks of the cells;

(b) cumulatively storing the results of the serial matching of step (a) as the matching proceeds; and

(c) causing, during the access phase, the cells matched in the search phase to be serially available for access via the common address and data buses, said access phase occurring subsequent to said search phase.

14. (*New*) The method of claim **13**, further including determining which bits of the words of the sequence of words are used for matching in the search phase.

15. (*New*) The method of claim **13**, comprising the steps of choosing a standard byte address in all data blocks and including a

byte different from an inactive state of the data bus in that address in every data block.

16. (*New*) The method of claim **13**, further including choosing a standard byte address in all data blocks and filling the data blocks with one data value if the data block in that cell is valid and another data value if the data block in the cell is cleared.